ABSTRACT OF THE DISCLOSURE

A test pattern sequence is generated (101), then a logic simulation of the operation of an IC under test in the case of applying each test pattern of the test pattern sequence, and a logic signal value sequence occurring in each signal line of the IC under test (102). The logic signal value sequence in each signal line is used to register in a fault list parts (a logic gate, signal line or signal propagation path) in which a fault (a delay fault or an open fault) detectable by a transient power supply current testing using the test pattern sequence is likely to occur (103).